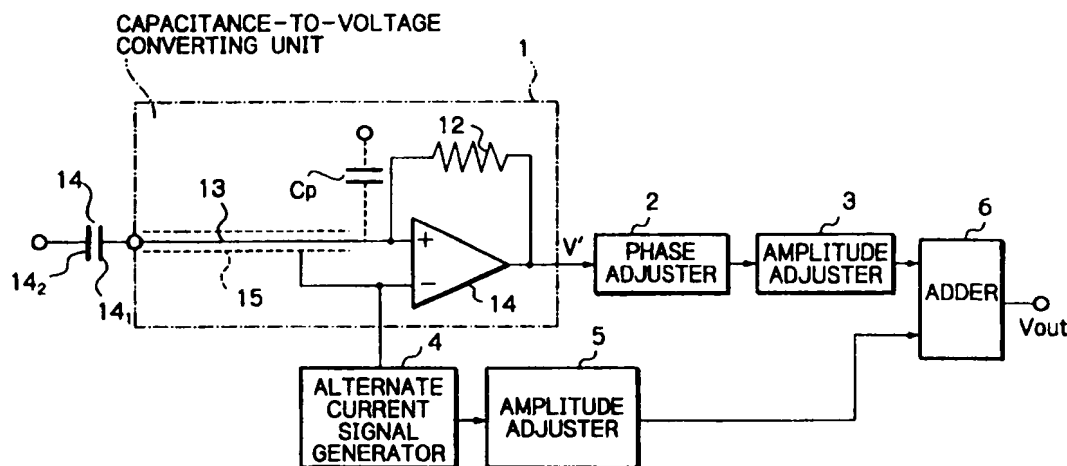




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(54) Title: STATIC CAPACITANCE-TO-VOLTAGE CONVERTER AND CONVERTING METHOD



(57) Abstract

A static capacitance-to-voltage converter is capable of converting a static capacitance into a voltage without suffering from a stray capacitance formed between a signal and a shielding line or a stray capacitance formed between an exposed portion of the signal line and its surroundings. The static capacitance-to-voltage converter is formed of an operational amplifier placed in an imaginary short-circuit state between an inverting input and a non-inverting input thereof; a signal line having one end connected to the inverting input and the other end capable of being connected to a static capacitance; a shielding line surrounding the signal line and connected to the non-inverting input; an alternate current signal generator for applying the non-inverting input with an alternate current signal; and zero adjusters for adjusting the output of the static capacitance-to-voltage converter to minimum when no static capacitance is connected to the signal line.

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DESCRIPTION

STATIC CAPACITANCE-TO-VOLTAGE
CONVERTER AND CONVERTING METHOD

TECHNICAL FIELD

5 The present invention relates to a static capacitance-to-voltage converter and an associated converting method which are capable of highly accurate conversion of a static capacitance into a corresponding voltage by eliminating the influence of a stray capacitance occurring on a signal line
10 for connecting the static capacitance to an operational amplifier.

BACKGROUND ART

 Fig. 1 generally illustrates the configuration of a static capacitance-to-voltage converter described in Laid-
15 open Japanese Patent Application No. 61-14578. This static capacitance-to-voltage converter has been proposed to solve a problem of the prior art which suffers from the inability of accurate voltage conversion due to the fact that a stray capacitance of a cable used to connect an unknown static
20 capacitance is superimposed on the unknown static capacitance, and that these static capacitances may vary due to movements and bending of the cable or the like. As illustrated in Fig. 1, an unknown capacitance C_x is connected between an alternate current (AC) signal generator
25 OS and an operational amplifier OP with connection cables covered with shielding lines ϕ to reduce the influence of stray capacitances C_{s1} , C_{s2} , C_{s3} . Specifically, an output and an inverting input of the operational amplifier OP are

connected through a feedback circuit formed of a parallel circuit including a resistor R_f and a capacitor C_f . The unknown capacitance C_x has one end connected to the inverting terminal of the operational amplifier OP through a
5 shielding line s , and the other end connected to the AC signal generator OS through another shielding line s . Both of the shielding lines and a non-inverting input of the operational amplifier OP are grounded.

With the configuration described above, since
10 substantially no voltage difference exists between the two ends of the unknown capacitance C_x , the stray capacitance C_{s2} is not charged. Also, since the stray capacitance C_{s3} is regarded as a coupling capacitance of both the shielding lines s , the stray capacitance C_{s3} can be eliminated by
15 grounding the shielding lines s . In this way, the influence exerted by the stray capacitances of the cables for connecting the unknown capacitance C_x is reduced by using the shielding lines s , so that a charge equal to that induced on the unknown static capacitance C_x is induced on
20 the capacitor C_f of the feedback circuit, resulting in an output proportional to the unknown static capacitance C_x produced from the operational amplifier OP. Stated another way, assuming that an output voltage of the AC signal generator OS is V_i , an output voltage V_o of the operational
25 amplifier OP is expressed by $-(C_x/C_f)V_i$, so that the converter of Fig. 1 may be used to convert the unknown static capacitance C_x into the voltage V_o from which the unknown static capacitance C_x can be derived together with

the known values C_f and V_i .

SUMMARY OF THE INVENTION

The static capacitance-to-voltage converter illustrated in Fig. 1, however, implies a problem that as
5 the unknown static capacitance C_x is smaller, the influence of stray capacitances becomes prominent, so that the static capacitance C_x cannot be accurately converted into a voltage.

In addition, since the feedback circuit of the operational amplifier OP is formed of a parallel circuit including the
10 resistor R_f and the capacitor C_f , separate steps are required to form a resistor and a capacitor for actually integrating necessary components into a converter in a one-chip form, causing disadvantages of a complicated manufacturing process and an increased chip size. Furthermore,
15 since the capacitor cannot be applied with an AC signal when one electrode of the static capacitance C_x is being biased at a certain voltage, a conversion of the static capacitance into an output voltage cannot be performed.

To solve the problem as mentioned, the applicant has
20 proposed a static capacitance-to-voltage converter constructed as illustrated in Fig. 2. In the following, this static capacitance-to-voltage converter will be described in detail with reference to Fig. 2. An operational amplifier 21 has a voltage gain extremely larger
25 than a closed loop gain. A gain seems to be almost infinity. A feedback resistor 23 is connected between an output terminal 22 and an inverting input terminal (-) of the operational amplifier 21 to form a negative feedback for

the operational amplifier 21. The operational amplifier 21 has a non-inverting input terminal (+) connected to an alternate current (AC) signal generator 24 and the inverting input terminal (-) connected to one end of a signal line 25 which has the other end connected to one electrode 26₁ of a capacitor 26 having an unknown or known static capacitance. The other electrode 26₂ of the capacitance 26 is grounded, clamped to a fixed direct current (DC) bias voltage or not grounded. The other electrode 26₂ may be applied with an AC bias. In this case, the bias current may have a frequency identical to or different from the frequency of an AC signal output from the AC signal generator 24.

The signal line 25 is surrounded by a shielding line 27 for preventing unwanted signals such as noise from being induced into the signal line 25 from the outside. The shielding line 27 is not grounded but is connected to the non-inverting input terminal (+) of the operational amplifier 21.

Since the operational amplifier 21 is formed with a negative feedback through the feedback resistor 23, and the operational amplifier 21 has a voltage gain extremely larger than a closed loop gain, the operational amplifier 21 is in an imaginary short-circuit state, and a gain seems to be almost infinity. In other words, an electric potential difference between the inverting input terminal (-) and the non-inverting input terminal (+) of the operational amplifier 21 is substantially zero. Thus, since the signal line 25 and the shielding line 27 are at the same voltage,

it is possible to cancel a stray capacitance possibly occurring between the signal line 25 and the shielding line 27. This holds true irrespective of the length of the signal line 25, and also holds true irrespective of
5 movements, bending, folding and so on of the signal line 25.

Assume now that an AC output voltage of the AC signal generator 24 is V_i ; its angular frequency is ω ; the static capacitance of the capacitor 26 is C_x ; a current flowing through the capacitance 26 is i_1 ; the resistance of the
10 feedback resistor 23 is R_f ; a current flowing through the feedback resistor 23 is i_2 ; a voltage at the inverting input terminal of the operational amplifier 21 is V_m ; an output voltage of the operational amplifier 21 is V , the voltage V_m at the inverting input terminal (-) is at the same voltage
15 as the AC signal output voltage V_i of the AC signal generator 24 since the operational amplifier 21 is in an imaginary short-circuit state, as mentioned above. That is, the following equation is satisfied:

$$V_i = V_m$$

20 In addition, the following equations are also satisfied:

$$i_1 = -V_m / (1/j\omega C_x) = -V_i / (1/j\omega C_x)$$

$$i_2 = (V_m - V) / R_f = (V_i - V) / R_f$$

Here, since $i_1 = i_2$, the output voltage V of the operational
25 amplifier 21 is expressed by the following equation:

$$V = V_i(1 + j\omega R_f \cdot C_x)$$

This equation indicates that the output voltage V of the operational amplifier 21 includes an AC component

proportional to the static capacitance C_x . It is therefore possible to derive a DC voltage proportional to the static capacitance C_x by appropriately processing the output voltage V .

5 As described above, since the operational amplifier 21 is in an imaginary short-circuit state so that a stray capacitance occurring between the signal line 25 and the shielding line 27 will not appear between the inverting input terminal (-) and the non-inverting input terminal (+)
10 of the operational amplifier 21, the equation representing the output voltage V of the operational amplifier 21 does not include a term related to the stray capacitance occurring between the signal line 25 and the shielding line 27. For this reason, a very small static capacitance C_x can
15 be converted into a voltage. In addition, even if the AC output voltage V_i has a low angular frequency ω , a voltage V exactly corresponding to the static capacitance C_x can be output.

 In the static capacitance-to-voltage converter of Fig.
20 2, since the signal line 25 and one end of the feedback resistor 23 are connected to the inverting input terminal (-) of the operational amplifier 21, the signal line 25 inevitably includes a portion left exposed, without being surrounded by the shielding line 27, near the end connected
25 to the inverting input terminal. Since a stray capacitance is formed between the exposed portion of the signal line 25 and its surroundings, the influence of this stray capacitance becomes sometimes more prominent as the static

capacitance C_x is smaller, causing a problem that an accurate detection of the static capacitance C_x is prevented.

The present invention has been proposed to solve the problems mentioned above, and it is therefore an object of the present invention to provide an impedance-to-voltage converter and an associated converting method which are capable of highly accurate conversion of an impedance of an object under measurement into a corresponding voltage by utilizing an operational amplifier in an imaginary short-circuit state to eliminate the influence of a stray capacitance between a line connected to a non-inverting terminal of the operational amplifier and a shielding line surrounding the line, and eliminating the influence of a stray capacitance formed by an unshielded portion of the signal line.

To achieve the above object, the present invention provides a static capacitance-to-voltage converter comprising:

an operational amplifier having an inverting input terminal, a non-inverting input terminal and an output terminal, wherein the operational amplifier has the output terminal and the inverting input terminal connected through a feedback resistor, and operable in an imaginary short-circuit state between the inverting input terminal and the non-inverting input terminal;

a signal line having one end connected to the inverting input terminal and the other end capable of being connected to a static capacitance element having a static

capacitance;

a shield surrounding at least a portion of the signal line, and connected to the non-inverting input terminal;

alternate current signal generator for applying the
5 non-inverting input terminal with an alternate current signal; and

an adjuster connected to the output terminal of the operational amplifier and an output terminal of the alternate current signal generator for adjusting an output
10 of the static capacitance-to-voltage converter to minimum (almost equal to zero) when no static capacitance element is connected to the signal line.

The adjuster comprises a variable frequency generator of the alternate current signal and an adjuster for
15 adjusting amplitudes and phases of an output signal of the operational amplifier and the alternate current signal such that they are canceled with each other.

The adjuster preferably comprises:

first adjuster for adjusting the amplitude of the
20 alternate current signal;

second adjuster for adjusting the phase and amplitude of an output voltage from the operational amplifier such the output voltage has the same amplitude as and an opposite phase to an output of the first adjuster; and

25 an adder for adding the output of the first adjuster and an output of the second adjuster.

Alternatively, the adjuster preferably comprises:

third adjuster for adjusting the amplitude of the

output voltage of the operational amplifier;

fourth adjuster for adjusting the phase and amplitude of the alternate current signal such that the alternate current signal has the same amplitude as and an opposite
5 phase to an output of the third adjuster; and

an adder for adding the output of the third adjuster and an output of the fourth adjuster.

Further, an integrator may be additionally provided for integrating an output of the adjuster, so that when a
10 static capacitance is connected to the other end of the signal line, a signal corresponding to the static capacitance of the static capacitance can be produced as an output of the integrator. Furthermore, a comparator may be provided for comparing the phase of the output of the
15 integrator with the phase of the alternate current signal. In this case, when a static capacitance is connected to the other end of the signal line, a signal representative of dielectric loss tangent for the static capacitance of the static capacitance can be produced as an output of the
20 comparator.

First and second synchronous detectors may further be provided for receiving the output of the integrator and the alternate current signal, such that the first synchronous detector outputs a signal representative of the static
25 capacitance of the static capacitance, and the second synchronous detector outputs a signal representative of dielectric loss tangent for the static capacitance of the static capacitance.

The present invention also provides a method of converting a static capacitance into a voltage comprising:

creating an imaginary short-circuit state between an inverting input terminal and a non-inverting input terminal
5 of an operational amplifier;

connecting one end of a signal line to the inverting input terminal, where the signal line has at least a portion thereof surrounded by a shield;

placing the shield at the same voltage as the non-inverting input terminal;
10

applying an alternate current signal to the non-inverting input terminal;

adjusting an output signal of the operational amplifier and the alternate current signal such that the output signal and the alternate current signal are canceled
15 with each other when no static capacitance is connected to the other end of the signal line; and

connecting a static capacitance to the other end of the signal line, after the adjusting an output signal of the operational amplifier and the alternate current signal such
20 that the output signal and the alternate current signal are canceled with each other when no static capacitance is connected to the other end of the signal line, to retrieve a voltage signal corresponding to the static capacitance of
25 the static capacitance.

Preferably, the adjusting an output signal of the operational amplifier and the alternate current signal such that the output signal and the alternate current signal are

canceled with each other when no static capacitance is connected to the other end of the signal line comprises:

varying the frequency of the alternate current signal;
and

- 5 adjusting the output signal of the operational amplifier and the alternate current signal in phase and amplitude such that the output signal and the alternate current signal are canceled with each other.

Also, the adjusting an output signal of the
10 operational amplifier and the alternate current signal such that the output signal and the alternate current signal are canceled with each other when no static capacitance is connected to the other end of the signal line may comprise:

adjusting the amplitude of the alternate current
15 signal;

adjusting the phase and amplitude of an output voltage from the operational amplifier such the output voltage has the same amplitude as and an opposite phase to the alternate current signal having its amplitude adjusted; and

- 20 adding the alternate current signal having its amplitude adjusted, and the output voltage of the operational amplifier having its phase and amplitude adjusted.

Alternatively, the adjusting an output signal of the
25 operational amplifier and the alternate current signal such that the output signal and the alternate current signal are canceled with each other when no static capacitance is connected to the other end of the signal line may comprise:

adjusting the amplitude of the output voltage of the operational amplifier;

adjusting the phase and amplitude of the alternate current signal such that the alternate current signal has
5 the same amplitude as and an opposite phase to the output voltage of the operational amplifier having its amplitude adjusted; and

adding the output voltage having its amplitude adjusted and the alternate current signal having its phase
10 and amplitude adjusted.

This converting method may also comprise:

integrating the voltage signal to output a signal corresponding to the static capacitance, and/or comparing the phase of the integrated signal with the phase of the
15 alternate current signal to output a signal representative of dielectric loss tangent for the static capacitance.

Furthermore, the integrated signal may be synchronously detected with the alternate current signal to output a signal representative of the static capacitance of
20 the static capacitance element and a signal indicative of dielectric loss tangent for the static capacitance of the static capacitance element.

The shield is preferably a shielding line surrounding the signal line over its entire length. Also, the static
25 capacitance may be a capacitive sensor. In addition, the static capacitance may comprise a measuring electrode so that a static capacitance is formed between an object under measurement and the measuring electrode.

Furthermore, during measurement waiting time, the measuring electrode may be accommodated in a case which is placed at the same voltage as a non-inverting input terminal of the operational amplifier, and a zero adjustment is performed to cancel a stray capacitance formed between the measuring electrode and its surroundings.

Since the operational amplifier is placed in an imaginary short-circuit state between the inverting input terminal and the non-inverting input terminal, a stray capacitance formed between the signal line and the shielding line is canceled. Also, by adjusting the static capacitance-to-voltage converter so that its output is minimum (almost equal to zero) when no static capacitance is connected to the signal line, the static capacitance-to-voltage converter is free from the influence of a stray capacitance formed by an exposed portion of the signal line.

Thus, a voltage corresponding to a static capacitance is output without suffering from such stray capacitances, however long the signal line and the shield are.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a schematic circuit diagram illustrating an example of a prior art static capacitance-to-voltage converter;

Fig. 2 is a schematic circuit diagram illustrating a static capacitance-to-voltage converter proposed by the applicant for solving drawbacks of the static capacitance-to-voltage converter of Fig. 1;

Fig. 3 is a block diagram generally illustrating the

configuration of a first embodiment of a static capacitance-to-voltage converter according to the present invention;

Fig. 4 is a circuit diagram illustrating an example of a specific configuration of the static capacitance-to-voltage converter of Fig. 3;

Fig. 5 is a block diagram illustrating the configuration of a capacitance meter which applies the static capacitance-to-voltage converter shown in Fig. 3;

Fig. 6 is a block diagram illustrating an example of a modification to the capacitance meter shown in Fig. 5;

Fig. 7 is a block diagram generally illustrating the configuration of a second embodiment of the static capacitance-to-voltage converter according to the present invention;

Fig. 8 is a circuit diagram illustrating an example of a specific configuration of the static capacitance-to-voltage converter of Fig. 7;

Fig. 9 is a block diagram illustrating the configuration of a capacitance meter which applies the static capacitance-to-voltage converter shown in Fig. 7; and

Fig. 10 is a block diagram illustrating an example of a modification to the capacitance meter shown in Fig. 9.

Fig. 11 shows an experimental result obtained from the example of a static capacitance-to-voltage converter shown in Fig. 4. In this example, suitable electric components are chosen in the electric circuits.

BEST MODE FOR CARRYING OUT THE INVENTION

The present invention will hereinafter be described in

detail in connection with preferred embodiments thereof with reference to the accompanying drawings. Fig. 3 is a block diagram generally illustrating a first embodiment of a static capacitance-to-voltage converter according to the present invention. Referring specifically to Fig. 3, the static capacitance-to-voltage converter comprises a capacitance-to-voltage converting unit 1; a phase adjuster 2 for adjusting the phase of an output voltage of the capacitance-to-voltage converting unit 1; a first amplitude adjuster 3 for adjusting the amplitude of a phase adjusted voltage; an alternate current (AC) signal generator 4 having a variable frequency generator; a second amplitude adjuster 5 for adjusting the amplitude of an AC signal from the AC signal generator 4; and an adder 6 for adding voltages output from the first amplitude adjuster 3 and the second amplitude adjuster 4.

The capacitance-to-voltage converting unit 1 includes an operational amplifier 11 which may be an amplifier having a voltage gain extremely larger than a closed loop gain. A gain seems to be almost infinity. A feedback resistor 12 is connected between an output and an inverting input terminal (-) of the operational amplifier 11 to form a negative feedback for the operational amplifier 11. The operational amplifier 11 has a non-inverting input terminal (+) applied with an AC signal from the AC signal generator 4, and the inverting input terminal (-) connected to one end of a signal line 13. The other end of the signal line 13 may be connected to a static capacitance element 14 having a static

capacitance C_x such as a capacitor or the like. The static capacitance element 14 includes one electrode 14_1 and the other electrode 14_2 , which is grounded, clamped to a fixed DC bias voltage, or not grounded. Alternatively, the other
5 electrode 14_2 may be applied with an AC bias having a frequency identical to or different from the frequency of the AC signal from the AC signal generator 4. While an ambient AC signal is further applied to the inverting input terminal (-) through a stray capacitance C_p , this AC signal
10 generally has a frequency which is different from that of the AC signal from the AC signal generator 4 and that of the AC bias applied to the electrode 14_2 .

The signal line 13 is surrounded by a shielding line 15 for preventing unwanted signals such as noise from being
15 induced into the signal line 13 from the outside. The shielding line 15 is not grounded but is connected to the non-inverting input terminal (+) of the operational amplifier 11.

The capacitance-to-voltage converting unit 1 has
20 substantially the same configuration as a static capacitance-to-voltage converter illustrated in Fig. 7. Specifically, since the operational amplifier 11 is formed with a negative feedback through the feedback resistor 12, the operational amplifier 11 has a voltage gain extremely
25 larger than a closed loop gain, and a gain seem to be almost infinity, the operational amplifier 11 is in an imaginary short-circuit state between both the input terminals thereof. In other words, a difference in voltage between the

inverting input terminal (-) and the non-inverting input terminal (+) of the operational amplifier 11 is substantially zero. Thus, since the signal line 13 and the shielding line 15 are at the same electric potential (so-called voltage), it is possible to cancel a stray capacitance possibly occurring between the signal line 13 and the shielding line 15. This holds true irrespective of the length of the signal line 13, and also holds true irrespective of movements, bending, folding and so on of the signal line 13.

However, since the signal line 13 has a portion near the end connected to the inverting input terminal (-) of the operational amplifier 11 left exposed, without being shielded by the shielding line 15, a stray capacitance C_p is formed between the exposed portion of the signal line 13 and its surroundings. This stray capacitance C_p adversely affects the output voltage of the operational amplifier 11 and hence an output voltage V' of the capacitance-to-voltage converting unit 1, with the result that the output voltage V' fails to accurately represent the static capacitance of the static capacitance element 14.

To eliminate the influence of the stray capacitance C_p , in the first embodiment of the present invention, the frequency of the AC signal output from the AC signal generator 4 is adjusted to reduce the output voltage V_{out} of the adder 6 to substantially zero when the static capacitance element 14 is not connected to the other end of the signal line 13, as well as the phase and amplitude of

the output voltage V' is adjusted by the phase adjuster 2 and the first amplitude adjuster 3, respectively, and the amplitude of the AC signal from the AC signal generator 4 is adjusted by the second amplitude adjuster 5 such that the
5 output of the first amplitude adjuster 3 has the same amplitude as and the opposite phase to the output of the second amplitude adjuster 5. Then, the two outputs are added by the adder 6. In this way, the outputs of the first amplitude adjuster 3 and the second amplitude adjuster 5 are
10 canceled.

Stated another way, a variable frequency generator of the AC signal generator 4, the phase adjuster 2, the first amplitude adjuster 3, the second amplitude adjuster 5, and the adder 6 constitute an adjuster which minimizes electric
15 potential difference or which adjusts electric potential difference. When the static capacitance element 14 is connected to the other end of the signal line 13 after minimizing or a zero adjustment has been made, a voltage V_{out} exactly corresponding to the static capacitance of the
20 static capacitance element 14 is output from the adder 6 without suffering from the influence of the stray capacitance C_p and a stray capacitance between the signal line 13 and the shielding line 15.

Fig. 4 is a circuit diagram illustrating an example of
25 the configuration and interconnections between various components of the static capacitance-to-voltage converter of Fig. 3. Fig. 4 shows resistors $R1 - R13$; a capacitor $C1$; operational amplifiers $AMP1 - AMP6$; an AC signal V_{in} having

an angular frequency ω ; and a bias voltage V_s which is applied to non-inverting input terminals of respective operational amplifiers in the phase adjuster 2, the first amplitude adjuster 3, the second amplitude adjuster 5 and the adder 6. It should be noted that the capacitance-to-voltage converting unit 1 in Fig. 4 is composed of the resistor R_1 representative of the feedback resistor 12 and the operational amplifier AMP1 representative of the operational amplifier 11. The AC signal generator 4 in turn is configured to apply the output V_{in} of an oscillator to a buffer including the operational amplifier AMP4 to produce an output voltage $V_d (=V_{in})$.

In the following, the operation of the static capacitance-to-voltage converter in Fig. 4 will be described from a mathematical viewpoint. Assume now that the output voltage of the capacitance-to-voltage converting unit 1 is V_a ; the output voltage of the phase adjuster 2 is V_b ; the output voltage of the first amplitude adjuster 3 is V_c ; the output voltage of the AC signal generator 4 is V_d ; the output voltage of the second amplitude adjuster 5 is V_e ; and $R_3=R_4$. Further, assuming $V_s=0$ for simplifying the calculation, the following equation is satisfied:

$$V_a = V_{in}[1+R_1 \cdot j\omega(C_x+C_p)]$$

$$V_b = V_a(1-R_5 \cdot j\omega C_1)/(1+r_5 \cdot j\omega C_1)$$

$$V_c = (R_7/R_6)V_b$$

$$V_d = V_{in}$$

$$V_e = (R_{11}/R_{10})V_{in}$$

$$V_{out} = -(R_9/R_8)V_c + [1+(R_9/R_8)] \times [R_{13}/(R_{12}+R_{13})]V_e$$

Therefore, the output voltage V_{out} of the adder 6 is expressed by the following equation:

$$\begin{aligned}
 V_{out} = & (R_9/R_8)(R_7/R_6) \\
 & \times \{ [1+R_1 \cdot j\omega(C_x+C_p)](1-R_5 \cdot j\omega C_1) \\
 & / (1+R_5 \cdot j\omega C_1) \} V_{in} \\
 & - \{ 1+(R_9/R_8)[R_{13}/(R_{12}+R_{13})] \} \\
 & \times (R_{11}/R_{10}) V_{in}
 \end{aligned}$$

Here, when the resistances are selected such that $R_1=R_2$, $R_6=R_7$, $R_8=R_9$, $R_{10}=2R_{11}$, $R_{12}=R_{13}$ are satisfied, the output voltage V_{out} of the adder 6 can be rewritten as follows:

$$\begin{aligned}
 V_{out} = & \{ [1+R_1 \cdot j\omega(C_x+C_p)](1-R_5 \cdot j\omega C_1) / \\
 & (1+R_5 \cdot j\omega C_1) \} V_{in} - 2V_{in} \quad (1)
 \end{aligned}$$

In the present invention, first, when the static capacitance element 14 is not connected to the signal line 13, i.e., when $C_x=0$, the phase and amplitude of the output voltage of the capacitance-to-voltage converting unit 1 and the angular frequency and amplitude of the AC signal output from the AC signal generator 4 are adjusted such that V_{out} in the equation (1) is zero. Substituting $V_{out}=0$ in the equation (1) for finding a condition in which V_{out} is zero, the following equation is derived:

$$\begin{aligned}
 & \{ [1+R_1 \cdot j\omega(C_p)](1-R_5 \cdot j\omega C_1) / \\
 & (1+R_5 \cdot j\omega C_1) \} - 2 = 0
 \end{aligned}$$

This equation is rewritten in the following form:

$$R_1 R_5 \omega^2 C_1 C_p - 1 + (R_1 C_p - 3 R_5 C_1) j\omega = 0$$

To satisfy this equation, the following conditions must be met:

$$R_1 R_5 \omega^2 C_1 C_p = 1 \quad (2)$$

$$R1Cp = 3R5C1 \quad (3)$$

Thus, substituting the equation (3) into the equation (2), and solving the equation (2) for ω ,

$$\begin{aligned} \omega &= 1/(R1CpR5C1)^{1/2} \\ 5 \quad &= 1/[(3)^{1/2}R5C1] \quad (4) \end{aligned}$$

is derived.

As will be understood from the foregoing, in the present invention, R5, C1 and ω are adjusted so as to satisfy the equations (3) and (4) in a state in which the static capacitance element 14 is not connected to the signal 10 13, so that the output voltage Vout of the adder 6 becomes zero.

Next, when the static capacitance element 14 is connected to the signal line 13, the following equation is 15 satisfied as mentioned above:

$$\begin{aligned} & \{[1+R1 \cdot j\omega(Cp)](1-R5 \cdot j\omega C1) / \\ & (1+R5 \cdot j\omega C1)\} Vin - 2Vin = 0 \end{aligned}$$

Further, since the equations (3) and (4) are satisfied, the equation (1) can be rewritten as follows:

$$\begin{aligned} 20 \quad Vout &= R1 \cdot j\omega Cx (1-R5 \cdot j\omega C1) \\ & / (1+R5 \cdot j\omega C1) \end{aligned}$$

Substituting this into the equation (4), Vout is expressed as follows:

$$Vout = (4/3) Vin R1 \cdot j\omega Cx \quad (5)$$

25 This equation (5) indicates that the output voltage Vout of the adder 6 is not influenced at all by any static capacitance other than the static capacitance Cx of the static capacitance element 14.

As described above in detail, since the static capacitance-to-voltage converter illustrated in Figs. 3 and 4 cancels a stray capacitance formed between the signal line 13 and the shielding line 15, and a stray capacitance formed between the exposed portion of the signal line 13 and its surroundings, it can output a voltage exactly corresponding to the static capacitance C_x of the static capacitance element 14 without suffering from the influence of such stray capacitances.

In the description heretofore made, connecting the static capacitance element 14 having the static capacitance C_x to the signal line 13 is equivalent to a change in the static capacitance connected to the inverting input terminal of the operational amplifier AMP1 by C_x . Therefore, the static capacitance-to-voltage converter of Figs. 3 and 4 can also output a voltage exactly corresponding to ΔC_x when the static capacitance C_x of the static capacitance element 14 connected to the signal line 13 has changed by ΔC_x . In the following, this operation will be described in detail in connection with the static capacitance-to-voltage converter of Fig. 4.

The output voltage V_{out} of the adder 6 when the static capacitance element 14 is connected to the signal line 13 is expressed by the aforementioned equation (1). Assume that V_{out} is zero in this condition. Conditions for satisfying this can be found by giving $V_{out}=0$ in the equation (1):

$$R5C1 = (1/3)R1(Cx+Cp) \quad (6)$$

$$\omega = 1/(3)^{1/2} R5C1 \quad (7)$$

Stated another way, the output voltage V_{out} of the adder 6 can be made zero by adjusting the angular frequency ω of the AC signal from the AC signal generator 4, R_5 and C_1 to satisfy the equations (6) and (7).

- 5 Next, the output voltage V_{out} of the adder 6, when the static capacitance C_x of the static capacitance element 14 has changed by ΔC_x , can be expressed by substituting $C_x + \Delta C_x$ for C_x in the equation (1):

$$\begin{aligned} V_{out} = & \{ [1 + R_1 \cdot j\omega(C_x + \Delta C_x + C_p)] \\ 10 \quad & \times (1 - R_5 \cdot j\omega C_1) / (1 + R_5 \cdot j\omega C_1) \} V_{in} \\ & - 2V_{in} \end{aligned} \quad (8)$$

Then, substituting the equations (6) and (7) into the equation (8), and using $V=0$ in the equation (1):

$$V_{out} = (4/3)V_{in}R_1 \cdot j\omega \Delta C_x \quad (9)$$

- 15 This equation indicates that V_{out} exactly corresponds to ΔC_x .

This also indicates that the static capacitance-to-voltage converter of Fig. 4 is capable of outputting a voltage exactly corresponding to a change in capacitance of the static capacitance element 14 connected to the signal line

- 20 13.

While the foregoing description has been made on the assumption that $V_s=0$ is satisfied, the same conclusion is derived also when $V_s \neq 0$, only except that associated calculations are more complicated. Alternatively, in Figs.

25 3 and 4, a subtractor may be used in place of the adder 6 such that the subtractor is applied with the output of the first amplitude adjuster 3 and the output of the second amplitude adjuster 5 which are adjusted to have the same

amplitude and the same phase.

Next, a capacitance meter, which is an exemplary application of the static capacitance-to-voltage converter illustrated in Fig. 3, will be described with reference to Fig. 5. This capacitance meter is configured such that an integrator 16 is connected additionally to the adder in Fig. 3, and outputs of the integrator 16 and the AC signal generator 4 are connected to a phase comparator 17.

As mentioned above, the output voltage V_{out} of the adder 6 is expressed by the equations (5) and (9). By integrating this voltage by the integrator 16, it is possible to produce a voltage E which is proportional to the static capacitance C_x of the static capacitance element 14 or a change ΔC_x in the static capacitance C_x . Also, by using the phase comparator 17 to derive a difference in phase between the voltage E output from the integrator 16 and the AC signal V_{in} output from the AC signal generator 4, dielectric loss tangent can be derived for the static capacitance element 14.

In a manner similar to the foregoing, the capacitance meter illustrated in Fig. 5 may also be designed such that one electrode 14_1 of the static capacitance element 14 is used as a measuring electrode, and the other electrode 14_2 is used as an object under measurement for which a determination is made as to whether it is good or bad based on the magnitude of a static capacitance C_x formed between the one electrode 14_1 and the other electrode 14_2 . In this case, a housing for the capacitance meter is provided with a

case having the same electric potential (so-called voltage) as the operational amplifier 11. After the measuring electrode is accommodated in this case, the output voltage V_{out} of the adder 6 is adjusted to a minimum or zero. In this event, if the measuring electrode is taken out of the case during a measurement, the adder 6 experiences a drift by a voltage proportional to a stray capacitance between the measuring electrode and its surroundings. Therefore, a static capacitance between the measuring electrode and the object under measurement can be more accurately measured by correcting the phase adjuster 2, the first amplitude adjuster 3 and the second amplitude adjuster 5 such that the drift value becomes minimum or zero. When a measurement was actually made using a semiconductor device made of silicon, the capacitor meter was able to measure a very small static capacitance on the order of 1 femtofarad to 2 femtofarad, thereby demonstrating that the present invention is significantly effective.

Fig. 6 is a block diagram generally illustrating an exemplary modification to the capacitor meter illustrated in Fig. 5, where the output of the integrator 16 in Fig. 5 is connected to a first synchronous detector 18 and a second synchronous detector 19, such that these synchronous detectors 18, 19 are applied with an AC signal from an AC signal generator 4. When the first synchronous detector 18 synchronously detects a voltage E output from the integrator 16 with the AC signal V_{in} which is in phase with the voltage E , the static capacitance C_x of a static capacitance element

14 or a change ΔC_x in the static capacitance C_x can be derived as an output of the first synchronous detector 18. Similarly, when the second synchronous detector 19 synchronously detects the voltage E from the integrator 16 with the AC signal V_{in} which is out of phase by 90° from the voltage E , dielectric loss tangent for the static capacitance element 14 can be derived as an output of the second synchronous detector 19.

More specifically, the static capacitance C_x of the static capacitance element 14 can be derived by the first synchronous detector 18 as an average value or an integrated value of the voltage E over a range from 0° to 180° with respect to the phase of the AC signal V_{in} from the AC signal generator 4. Also, the dielectric loss tangent for the static capacitance C_x of the static capacitance element 14 can be derived by the second synchronous detector 19 as an average value or an integrated value of the voltage E over a range from 90° to 270° with respect to the phase of the AC signal V_{in} from the AC signal generator 14.

Next, a second embodiment of the static capacitance-to-voltage converter according to the present invention will be described with respect to the configuration with reference to Fig. 7. The second embodiment illustrated in Fig. 7 differs from the first embodiment illustrated in Fig. 3 in that the phase adjuster 2 is not connected between the capacitance-to-voltage converting unit 1 and the first amplitude adjuster 3, but between the AC voltage generator 4 and the second amplitude adjuster 5. While in the layout

illustrated in Figs. 3 and 4, high harmonic components of the AC signal V_{in} output from the AC signal generator 4 may be introduced into the phase adjuster 2 or the first amplitude adjuster 3, such an inconvenience can be

5 effectively prevented by connecting the phase adjuster 2 between the AC signal generator 4 and the second amplitude adjuster 5, as illustrated in Fig. 7.

Fig. 8 is a circuit diagram illustrating an example of the configuration of each component in the static

10 capacitance-to-voltage converter of Fig. 7 and interconnections between these components, wherein components identical or similar to those illustrated in Fig. 4 are designated the same reference numerals. Note, however, that the configuration of the first amplitude adjuster 3 is

15 modified such that the output of the capacitance-to-voltage converting unit 1 is connected to the non-inverting input terminal of the operational amplifier AMP3 through a resistor $R6'$, and an AC bias voltage V_s is applied to the inverting input terminal of the operational amplifier AMP3

20 through a resistor $R7'$.

In the following, the operation of the static capacitance-to-voltage converter of Fig. 8 will be described from a mathematical viewpoint. In Fig. 8, the following equations are satisfied:

$$\begin{aligned}
 25 \quad V_a &= V_{in}[1+R1 \cdot j\omega(Cx+Cp)] \\
 V_b &= V_{in} \\
 V_c &= (R7/R6)V_{in}+[1+(R7/R6)] \\
 &\quad \times [R7'/(R6'+R7')]V_a
 \end{aligned}$$

$$V_d = [(1+R_4/R_3)/(1+R_5 \cdot j\omega C_1) - R_4/R_3] V_b$$

$$V_e = (R_{11}/R_{10}) V_d$$

$$V_{out} = -(R_9/R_8) V_c + [1 + (R_9/R_8)]$$

$$5 \quad x [R_{13}/(R_{12}+R_{13})] V_e]$$

Therefore, the output voltage V_{out} of the adder 6 is expressed by the following equation:

$$\begin{aligned} V_{out} = & (R_9/R_8)(R_7/R_6) V_{in} - \{ [1 + R_7/R_6] \\ & x [R_7'/(R_6' + R_7')] [1 + R_1 \cdot j\omega (C_x \\ 10 \quad & + C_p)] \} V_{in} - \{ [1 + (R_9/R_8)] \\ & x [R_{15}/(R_{12}/R_3)] (R_{11}/R_{10}) \\ & x [1 + (R_4/R_3)] / (1 + R_5 \cdot j\omega C_1) \\ & - (R_4/R_3) \} V_{in} \end{aligned}$$

Here, when the resistances are selected such that $R_3=R_4$,
 15 $R_6=R_7$, $R_6'=R_7'$, $R_8=R_9$, $R_{10}=R_{11}$, and $R_{12}=R_{13}$ are satisfied, the output voltage V_{out} of the adder 6 can be rewritten as follows:

$$\begin{aligned} V_{out} = & \{ [R_5 \cdot j\omega C_1 - 1] / (1 + R_5 \cdot j\omega C_1) \} \\ & - R_1 \cdot j\omega (C_x + C_p) \} V_{in} \end{aligned} \quad (10)$$

20 When the static capacitance element 14 is not connected to the signal line 13, i.e., when $C_x=0$, the amplitude of the output voltage of the capacitance-to-voltage converting unit 1 and the angular frequency, amplitude and phase of the AC signal output from the AC
 25 signal generator 4 are adjusted such that V_{out} in the equation (10) is zero. Substituting 0 into V_{out} ($V_{out}=0$) and 0 into C_x ($C_x=0$) in the equation (10) for finding a condition in which V_{out} is zero, the equation (10) can be

rewritten as follows:

$$[(R5 \cdot j\omega C1 - 1) / (1 + R5 \cdot j\omega C1)] - R1 \cdot j\omega C_p = 0 \quad (11)$$

From this equation,

$$R5C1 = R1C_p \quad (12)$$

$$5 \quad \omega = 1 / (R5C1R1C_p)^{1/2} \quad (13)$$

are derived. Thus, V_{out} can be made zero by adjusting $R5$, $C1$ and ω , so as to satisfy the equations (12) and (13) in a state in which the static capacitance element 14 is not connected to the signal line 13.

10 Next, when the static capacitance element 14 is connected to the signal line 13, the equation (10) can be rewritten as follows since the equations (11), (12) and (13) are satisfied as mentioned above:

$$V_{out} = V_{in} R1 \cdot j\omega C_x \quad (14)$$

15 This equation (14) indicates that the output voltage V_{out} of the adder 6 is not influenced at all by any static capacitance other than the static capacitance C_x of the static capacitance element 14.

20 As described above in detail, since the static capacitance-to-voltage converter according to the second embodiment illustrated in Figs. 7 and 8 also cancels a stray capacitance formed between the signal line 13 and the shielding line 15, and a stray capacitance formed between the exposed portion of the signal line 13 and its
25 surroundings, it can output a voltage exactly corresponding to the static capacitance C_x of the static capacitance element 14 without suffering from the influence of such stray capacitances.

In the description heretofore made in connection with the static capacitance-to-voltage converter of Fig. 8, connecting the static capacitance element 14 having the static capacitance C_x to the signal line 13 is equivalent to
 5 a change in the static capacitance connected to the inverting input terminal of the operational amplifier AMP1 by C_x . Therefore, the static capacitance-to-voltage converter of Fig. 8 can also output a voltage exactly corresponding to ΔC_x when the static capacitance C_x of the
 10 static capacitance element 14 connected to the signal line 13 has changed by ΔC_x . In the following, this operation will be described in detail.

The output voltage V_{out} of the adder 6 when the static capacitance element 14 is connected to the signal line 13 is
 15 expressed by the aforementioned equation (10). Assume that V_{out} is zero in this state. Conditions for satisfying this can be found by substituting 0 into V_{out} ($V_{out}=0$) in the equation (10):

$$R5C1 = R1(C_x + C_p) \quad (15)$$

$$\begin{aligned} \omega &= 1/[R5C1R1(C_x + C_p)]^{1/2} \\ &= 1/R5C1 \end{aligned} \quad (16)$$

Stated another way, the output voltage V_{out} of the adder 6 can be made zero by adjusting the angular frequency ω of the AC signal from the AC signal generator 4, R5 and C1 to
 25 satisfy the equations (15) and (16).

Next, the output voltage V_{out} of the adder 6, when the static capacitance C_x of the static capacitance element 14 has changed by ΔC_x , can be expressed by substituting $C_x + \Delta C_x$

for C_x in the equation (10):

$$V_{out} = \{[R_5 \cdot j\omega C_1 - 1] / (1 + R_5 \cdot j\omega C_1)] - R_1 \cdot j\omega (C_x + \Delta C_x + C_p)\} V_{in} \quad (17)$$

Then, substituting the equations (15) and (16) into the
 5 equation (17), and giving $V_{out}=0$ in the equation (17):

$$V_{out} = -V_{in} R_1 \cdot j\omega \Delta C_x \quad (18)$$

This equation indicates that V_{out} exactly corresponds to ΔC_x .
 This equation also indicates that the static capacitance-to-voltage converter of Fig. 8 is capable of outputting a
 10 voltage exactly corresponding to a change in capacitance of the static capacitance element 14 connected to the signal line 13.

While the foregoing description has also been made on the assumption that $V_s=0$ is satisfied, the same conclusion
 15 is, denied except when associated calculations are more complicated. Alternatively, in Figs. 7 and 8, a subtractor may be used in place of the adder 6 such that the subtractor is applied with the output of the first amplitude adjuster 3 and the output of the second
 20 amplitude adjuster 5 which are adjusted to have the same amplitude and the same phase.

Fig. 9 illustrates the configuration of a capacitance meter which applies the static capacitance-to-voltage converter illustrated in Fig. 7. This capacitance meter,
 25 similar to the capacitance meter illustrated in Fig. 5, has an integrator 16 connected to the adder 6, and outputs of the integrator 16 and the AC signal generator 4 connected to a phase comparator 17. While in the layout illustrated in

Figs. 3 and 4, high harmonic components of the AC signal V_{in} output from the AC signal generator 4 may be introduced into the phase adjuster 2 or the first amplitude adjuster 3, the introduction of such high harmonic components can be
5 effectively prevented by disposing the phase adjuster 2 at a position illustrated in Fig. 9.

As stated above, the output voltage V_{out} of the adder 6 is expressed by the equations (14) and (18). By integrating this voltage by the integrator 16, it is
10 possible to produce a voltage E which is proportional to the static capacitance C_x of the static capacitance element 14 or a change ΔC_x in the static capacitance C_x . Also, by using the phase comparator 17 to derive a difference in phase between the voltage E output from the integrator 16
15 and the AC signal V_{in} output from the AC signal generator 4, dielectric loss tangent can be derived for the static capacitance element 14.

In a manner similar to the capacitance meter of Fig. 5, the capacitance meter of Fig. 9 may also be designed such
20 that one electrode 14_1 of the static capacitance element 14 is used as a measuring electrode, and the other electrode 14_2 is used as an object under measurement for which a determination is made as to whether it is good or bad based on the magnitude of a static capacitance C_x formed between
25 the one electrode 14_1 and the other electrode 14_2 . In this case, a housing for the capacitance meter is provided with a case having the same electric potential (voltage) as the operational amplifier 11. After the measuring electrode is

accommodated in this case, the output voltage V_{out} of the adder 6 is adjusted to minimum or zero. In this event, if the measuring electrode is taken out of the case during a measurement, the adder 6 experiences a drift by a voltage proportional to a stray capacitance between the measuring electrode and its surroundings. Therefore, a static capacitance between the measuring electrode and the object under measurement can be more accurately measured by correcting the phase adjuster 2, the first amplitude adjuster 3 and the second amplitude adjuster 5 such that the drift value becomes minimum or zero. It is revealed from the foregoing that the capacitor meter of Fig. 9 is capable of measuring a very small static capacitance, as is the case of the capacitance meter of Fig. 5.

Fig. 10 is a block diagram generally illustrating an exemplary modification to the capacitor meter illustrated in Fig. 9, where the output of the integrator 16 in Fig. 9 is connected to a first synchronous detector 18 and a second synchronous detector 19, such that these synchronous detectors 18, 19 are applied with an AC signal V_{in} from an AC signal generator 4. When the first synchronous detector 18 synchronously detects a voltage E output from the integrator 16 with the AC signal V_{in} which is in phase with the voltage E , the static capacitance C_x of a static capacitance element 14 or a change ΔC_x in the static capacitance C_x can be derived as an output of the first synchronous detector 18. Similarly, when the second synchronous detector 19 synchronously detects the voltage E

from the integrator 16 with the AC signal V_{in} which is out of phase by 90° from the voltage E , dielectric loss tangent for the static capacitance element 14 can be derived as an output of the second synchronous detector 19.

5 More specifically, the static capacitance C_x of the static capacitance element 14 can be derived by the first synchronous detector 18 as an average value or an integrated value of the voltage E over a range from 0° to 180° with respect to the phase of the AC signal V_{in} from the AC signal
10 generator 4. Also, the dielectric loss tangent for the static capacitance C_x of the static capacitance element 14 can be derived by the second synchronous detector 19 as an average value or an integrated value of the voltage E over a range from 90° to 270° with respect to the phase of the AC
15 signal V_{in} from the AC signal generator 14.

 In the two embodiments described above, an example of the static capacitance element 14 having a static capacitance to be converted into a voltage may be a capacitive sensor which has one electrode connected to the
20 inverting input terminal (-) of the operational amplifier AMP1 of the capacitance-to-voltage converting unit 1 through the signal line 13, and the other electrode (or a counterpart corresponding thereto) grounded, clamped at an appropriate bias electric potential (voltage), or opened in
25 a space without being grounded. Such capacitive sensors may include all devices for detecting a static capacitance as well as known capacitive sensor such as an acceleration sensor, seismometer, pressure sensor, displacement sensor,

displacement meter, proximity sensor, touch sensor, ion sensor, humidity sensor, rain drop sensor, snow sensor, lightening sensor, alignment sensor, touch failure sensor, shape sensor, end point detecting sensor, vibration sensor, ultrasonic sensor, angular velocity sensor, liquid amount sensor, gas sensor, infrared sensor, radiation sensor, level meter, freezing sensor, moisture meter, vibration meter, charge sensor and printed board tester. In addition, the present invention may also be applied to a clamp-type voltage meter or the like which measures a voltage in a contactless form.

Also, in the first and second embodiments, one electrode 14₁ of the static capacitance element 14 may be used as a measuring electrode, while the other electrode 14₂ is used as an object under measurement for which a determination is made as to whether it is good or bad based on the magnitude of a static capacitance C_x formed between the one electrode 14₁ and the other electrode 14₂.

For the purpose of verifying the operation of the static capacitance-to-voltage converter, the static capacitance-to-voltage converter structured such as shown in Fig. 4 was formed to obtain a relation between the output voltage V_{out} (mV) and the static capacitance C_x (fF). As a result, a linear relation between C_x and V_{out} was obtained, and it was made sure that we could measure no more than 1 - 3 femtofarad, as shown in Fig. 4.

INDUSTRIAL APPLICABILITY

As will be apparent from the foregoing description

with reference to the illustrated embodiments, the present invention produces the following effects:

- (1) The static capacitance of a static capacitance element connected to a signal line can be converted into a voltage without suffering from the influence of a stray capacitance formed between the signal line and a shielding line surrounding the signal line or a stray capacitance formed between an exposed portion of the signal line and its surroundings to derive a voltage exactly corresponding to the static capacitance, thereby making it possible to make highly accurate conversion of the static capacitance of a static capacitance element into a voltage and detect the voltage even if the static capacitance is very small, for example, on the order of femtofarad (1/1000 of picofarad).
- (2) Even if an electrode of a static capacitance element, which is not connected to a signal line, is biased at a certain electric potential (voltage), it is possible to produce a voltage exactly corresponding to the static capacitance of the static capacitance element.
- (3) Since the static capacitance of a static capacitance element can be converted into a signal which includes the static capacitance and the frequency of an AC signal, the conversion of the static capacitance into a voltage and detection of the voltage can be achieved even if the AC signal has a low frequency under about 10 MHz..

CLAIMS

1. A static capacitance-to-voltage converter comprising:

an operational amplifier having an inverting input terminal, a non-inverting input terminal and an output

5 terminal, said operational amplifier having said output terminal and said inverting input terminal connected through a feedback resistor;

a signal line having one end connected to said inverting input terminal and the other end capable of being
10 connected to a static capacitance element having a static capacitance;

a shield surrounding at least a portion of said signal line, and connected to said non-inverting input terminal;

alternate current signal generator for applying said
15 non-inverting input terminal with an alternate current signal; and

an adjuster connected to the output terminal of said operational amplifier and an output terminal of said alternate current signal generator for adjusting an output
20 of said static capacitance-to-voltage converter to minimum when no static capacitance element is connected to said signal line.

2. A static capacitance-to-voltage converter comprising:

an operational amplifier having an inverting input
25 terminal, a non-inverting input terminal and an output terminal, said operational amplifier having said output terminal and said inverting input terminal connected through a feedback resistor;

a signal line having one end connected to said inverting input terminal and the other end capable of being connected to a static capacitance element having a static capacitance;

5 a shield surrounding at least a portion of said signal line, and connected to said non-inverting input terminal;

alternate current signal generator for applying said non-inverting input terminal with an alternate current signal;

10 a variable the frequency generator of said alternate current signal; and

an adjusting circuit for adjusting amplitudes and phases of an output signal of said operational amplifier and said alternate current signal such that they are canceled
15 with each other.

3. A static capacitance-to-voltage converter according to claim 2, wherein said adjusting circuit comprises:

first adjuster for adjusting the amplitude of said alternate current signal;

20 second adjuster for adjusting the phase and amplitude of an output voltage from said operational amplifier such said output voltage has the same amplitude as and an opposite phase to an output of said first adjuster; and

an adder for adding the output of said first adjuster
25 and an output of said second adjuster.

4. A static capacitance-to-voltage converter according to claim 2, wherein said adjusting circuit comprises:

third adjuster for adjusting the amplitude of the

output voltage of said operational amplifier;

fourth adjuster for adjusting the phase and amplitude of said alternate current signal such that said alternate current signal has the same amplitude as and an opposite

5 phase to an output of said third adjuster; and

an adder for adding the output of said third adjuster and an output of said fourth adjuster.

5. A static capacitance-to-voltage converter according to any of claims 1 - 4, further comprising integrator for
10 integrating an output of said adjuster, wherein when a static capacitance is connected to the other end of said signal line, a signal corresponding to the static capacitance of said static capacitance is produced as an output of said integrator.

15 6. A static capacitance-to-voltage converter according to claim 5, further comprising comparator for comparing the phase of the output of said integrator with the phase of said alternate current signal, wherein when a static capacitance is connected to the other end of said signal
20 line, a signal representative of dielectric loss tangent for the static capacitance of said static capacitance element is produced as an output of said comparator.

7. A static capacitance-to-voltage converter according to claim 5, further comprising first and second synchronous
25 detectors for receiving the output of said integrator and said alternate current signal, said first synchronous detector outputting a signal representative of the static capacitance of said static capacitance, and said second

synchronous detector outputting a signal representative of dielectric loss tangent for the static capacitance of said static capacitance.

8. A static capacitance-to-voltage converter according to
5 any of claims 1 - 7, wherein said shield surrounds said signal line over the entire length thereof.

9. A static capacitance-to-voltage converter according to any of claims 1 - 8, wherein said static capacitance is a capacitive sensor.

10 10. A static capacitance-to-voltage converter according to any of claims 1 - 9, wherein said static capacitance comprises a measuring electrode connected to the other end of said signal line so that a static capacitance is formed between an object under measurement and said measuring
15 electrode.

11. A static capacitance-to-voltage converter according to claim 10, further comprising a case placed at the same voltage as the non-inverting input terminal of said operational amplifier, for accommodating said measuring
20 electrode when no static capacitance is connected to said signal line, wherein said adjuster adjusts the output of said static capacitance-to-voltage converter to minimum when said measuring electrode is accommodated in said case.

12. A method of converting a static capacitance into a
25 voltage comprising:

connecting one end of a signal line to said inverting input terminal, said signal line having at least a portion thereof surrounded by a shield;

placing said shield at the same potential as said non-inverting input terminal;

applying an alternate current signal to said non-inverting input terminal;

5 adjusting an output signal of said operational amplifier and said alternate current signal such that said output signal and said alternate current signal are canceled with each other when no static capacitance is connected to the other end of said signal line; and

10 connecting a static capacitance to the other end of said signal line, after said adjusting, to retrieve a voltage signal corresponding to the static capacitance of said static capacitance.

13. A method of converting a static capacitance into a
15 voltage according to claim 12, wherein said adjusting an output signal of said operational amplifier and said alternate current signal such that said output signal and said alternate current signal are canceled with each other when no static capacitance is connected to the other end of
20 said signal line comprises:

varying the frequency of said alternate current signal; and

adjusting the output signal of said operational
amplifier and said alternate current signal in phase and
25 amplitude such that said output signal and said alternate current signal are canceled with each other.

14. A method of converting a static capacitance into a voltage according to claim 13, wherein said adjusting an

output signal of said operational amplifier and said
alternate current signal such that said output signal and
said alternate current signal are canceled with each other
when no static capacitance is connected to the other end of
5 said signal line comprises:

adjusting the amplitude of said alternate current
signal;

adjusting the phase and amplitude of an output voltage
from said operational amplifier such said output voltage has
10 the same amplitude as and an opposite phase to said
alternate current signal having its amplitude adjusted; and

adding said alternate current signal having its
amplitude adjusted, and the output voltage of said
operational amplifier having its phase and amplitude
15 adjusted.

15. A method of converting a static capacitance into a
voltage according to claim 13, wherein said adjusting an
output signal of said operational amplifier and said
alternate current signal such that said output signal and
20 said alternate current signal are canceled with each other
when no static capacitance is connected to the other end of
said signal line comprises:

adjusting the amplitude of an output voltage of said
operational amplifier;

25 adjusting the phase and amplitude of said alternate
current signal such that said alternate current signal has
the same amplitude as and an opposite phase to the output
voltage of said operational amplifier having its amplitude

adjusted; and

adding said output voltage having its amplitude adjusted and said alternate current signal having its phase and amplitude adjusted.

5 16. A method of converting a static capacitance into a voltage according to any of claims 12 - 15, further comprises integrating said voltage signal to output a signal corresponding to said static capacitance.

10 17. A method of converting a static capacitance into a voltage according to claim 16, further comprises comparing the phase of said integrated signal with the phase of said alternate current signal to output a signal representative of dielectric loss tangent for said static capacitance.

15 18. A method of converting a static capacitance into a voltage according to claim 16, further comprising synchronously detecting said integrated signal with said alternate current signal to output a signal representative of the static capacitance and a signal representative of dielectric loss tangent for the static capacitance.

20 19. A method of converting a static capacitance into a voltage according to any of claims 12 - 18, wherein said shield is a shielding line surrounding said signal line over its entire length.

25 20. A method of converting a static capacitance into a voltage according to any of claims 12 - 19, wherein said static capacitance is a capacitive sensor.

21. A method of converting a static capacitance into a voltage according to any of claims 12 - 20, wherein said

static capacitance comprises a measuring electrode so that a static capacitance is formed between an object under measurement and said measuring electrode.

22. A method of converting a static capacitance into a
5 voltage according to claim 21, further comprising:

accommodating said measuring electrode in a case during measurement waiting time, said case being placed at the same voltage as a non-inverting input terminal of said operational amplifier; and

10 performing a zero adjustment to cancel a stray capacitance formed between said measuring electrode and its ambient.

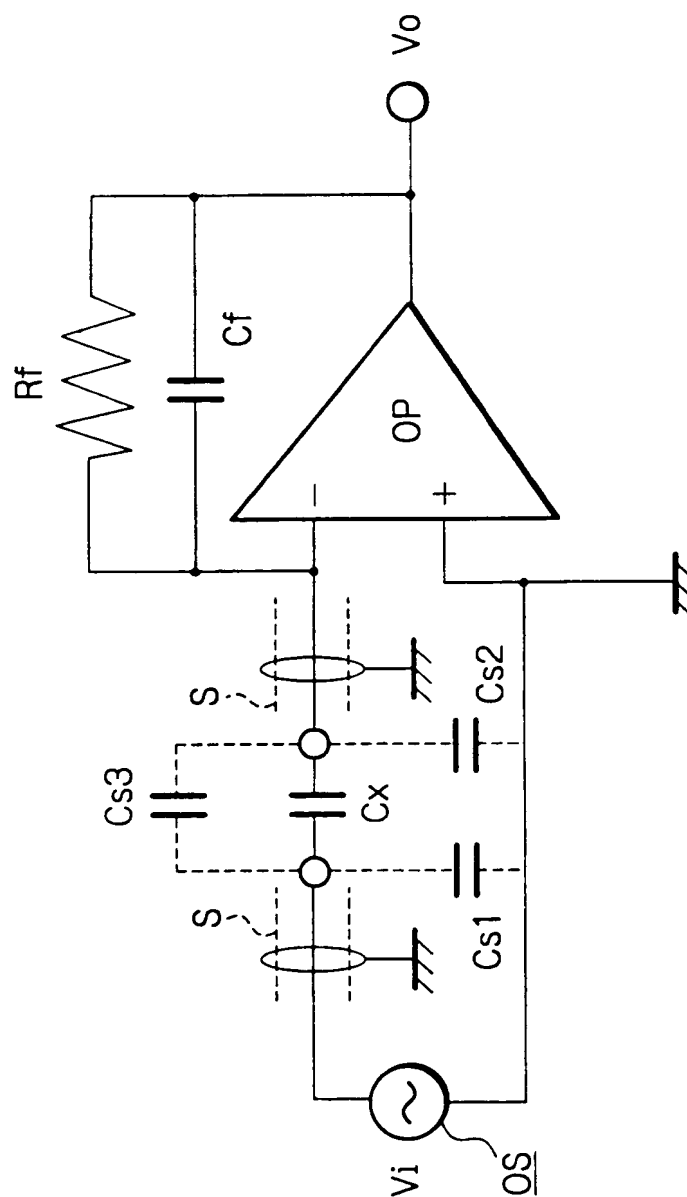
Fig. 1 (PRIOR ART)

Fig. 2

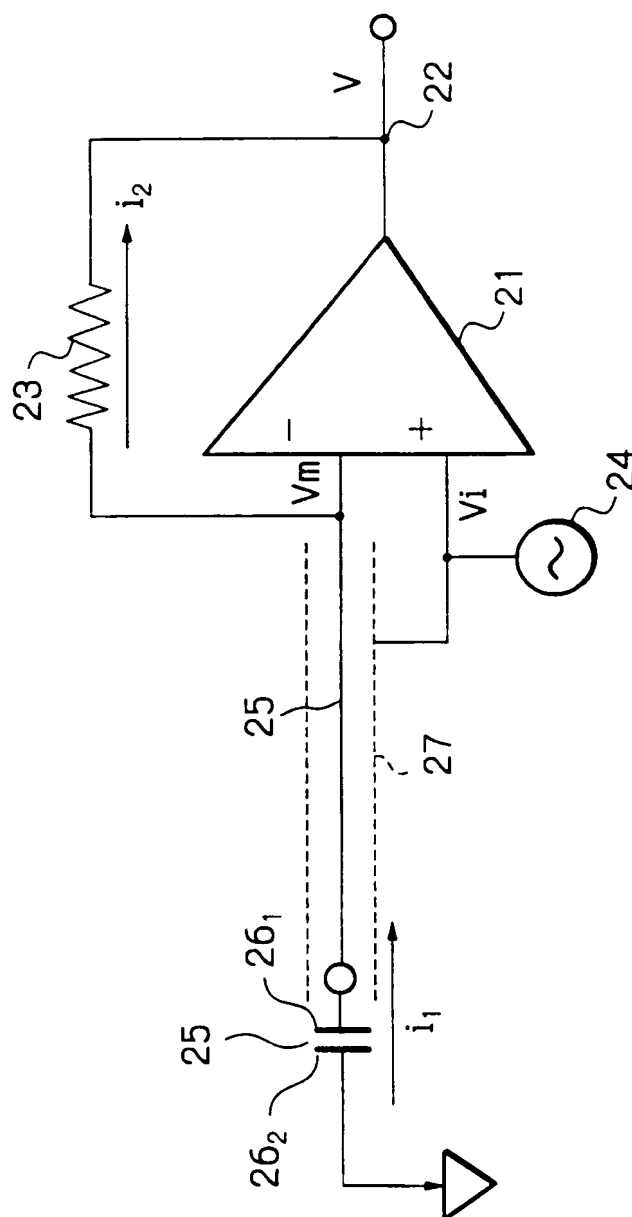


Fig. 3

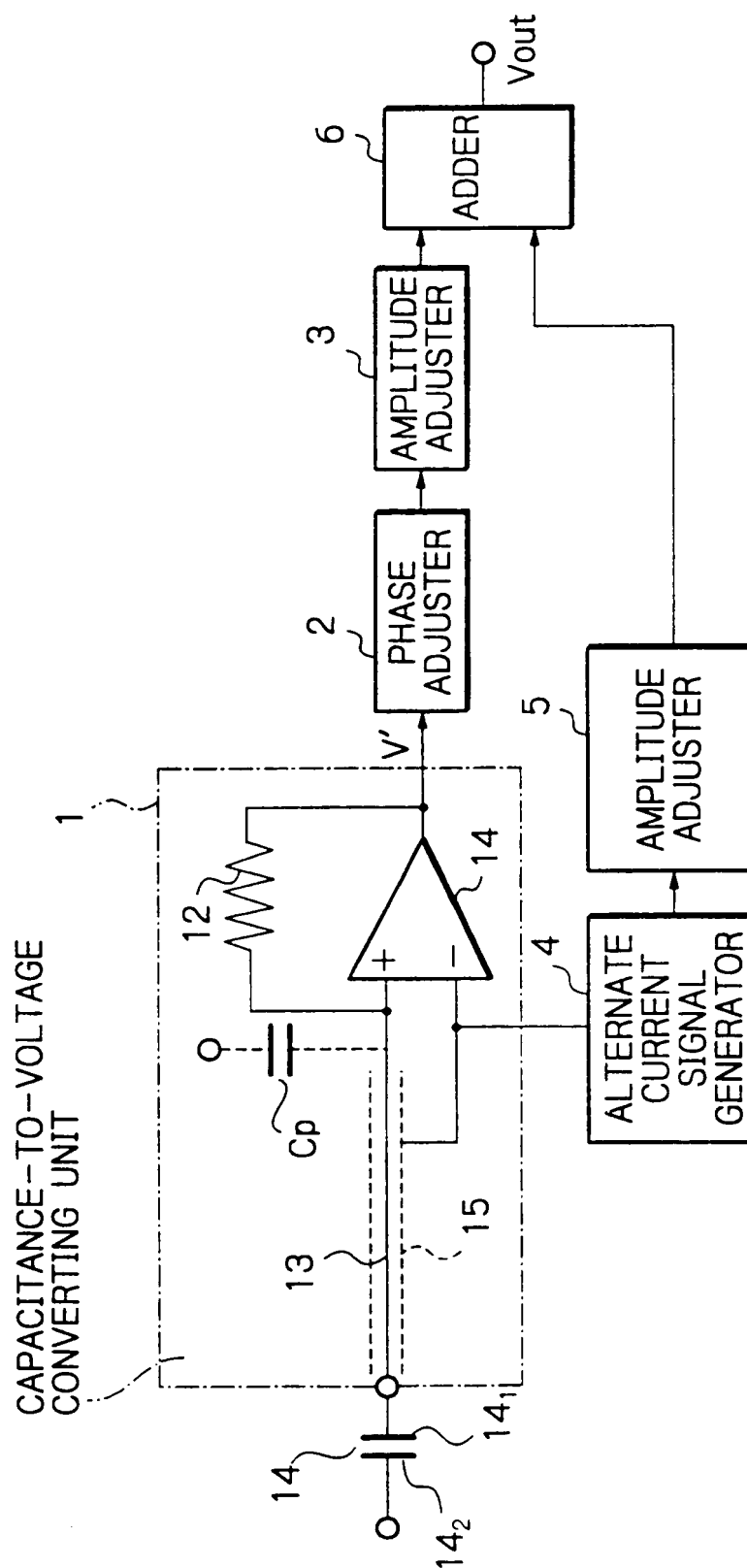


Fig. 4

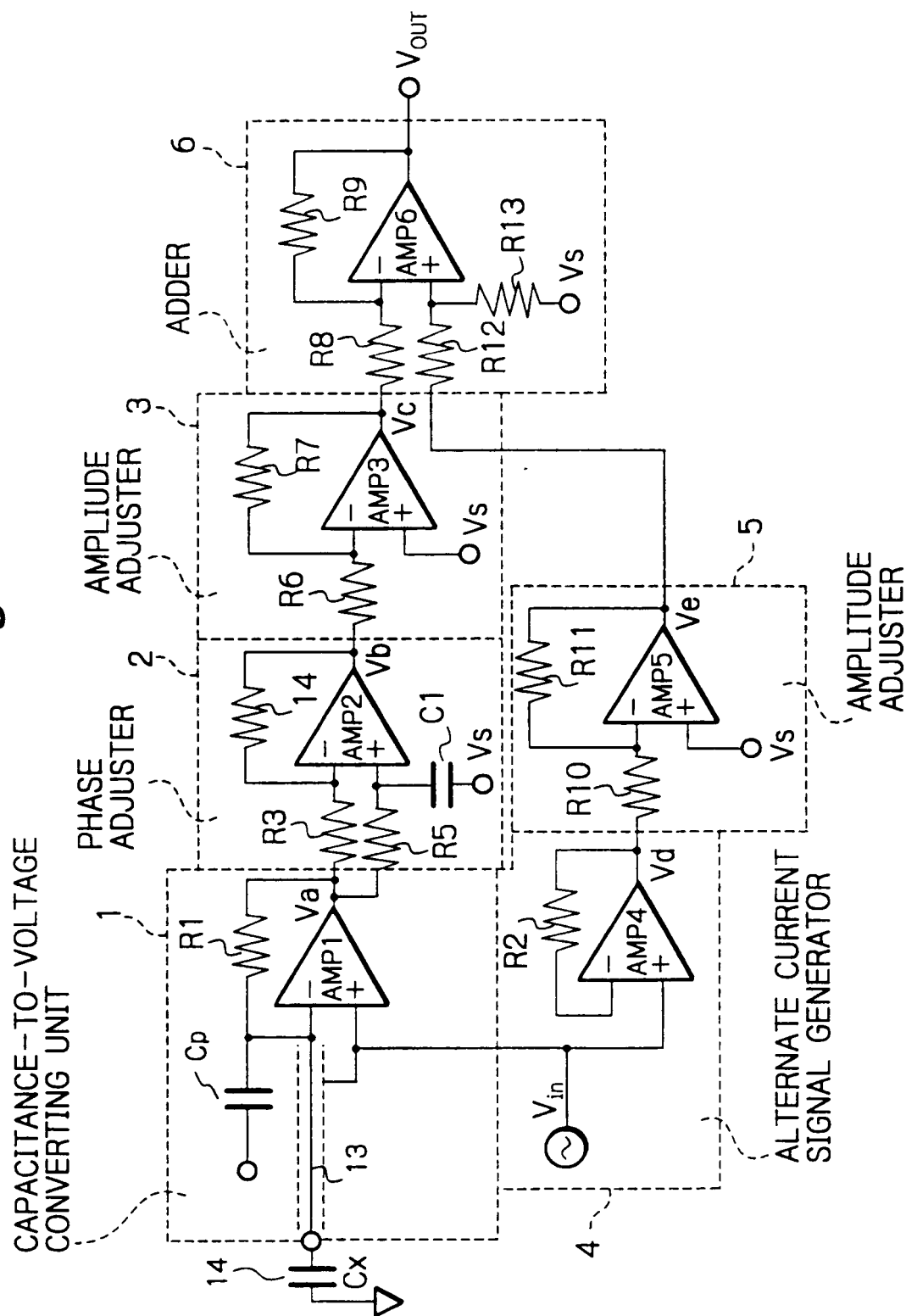


Fig. 5

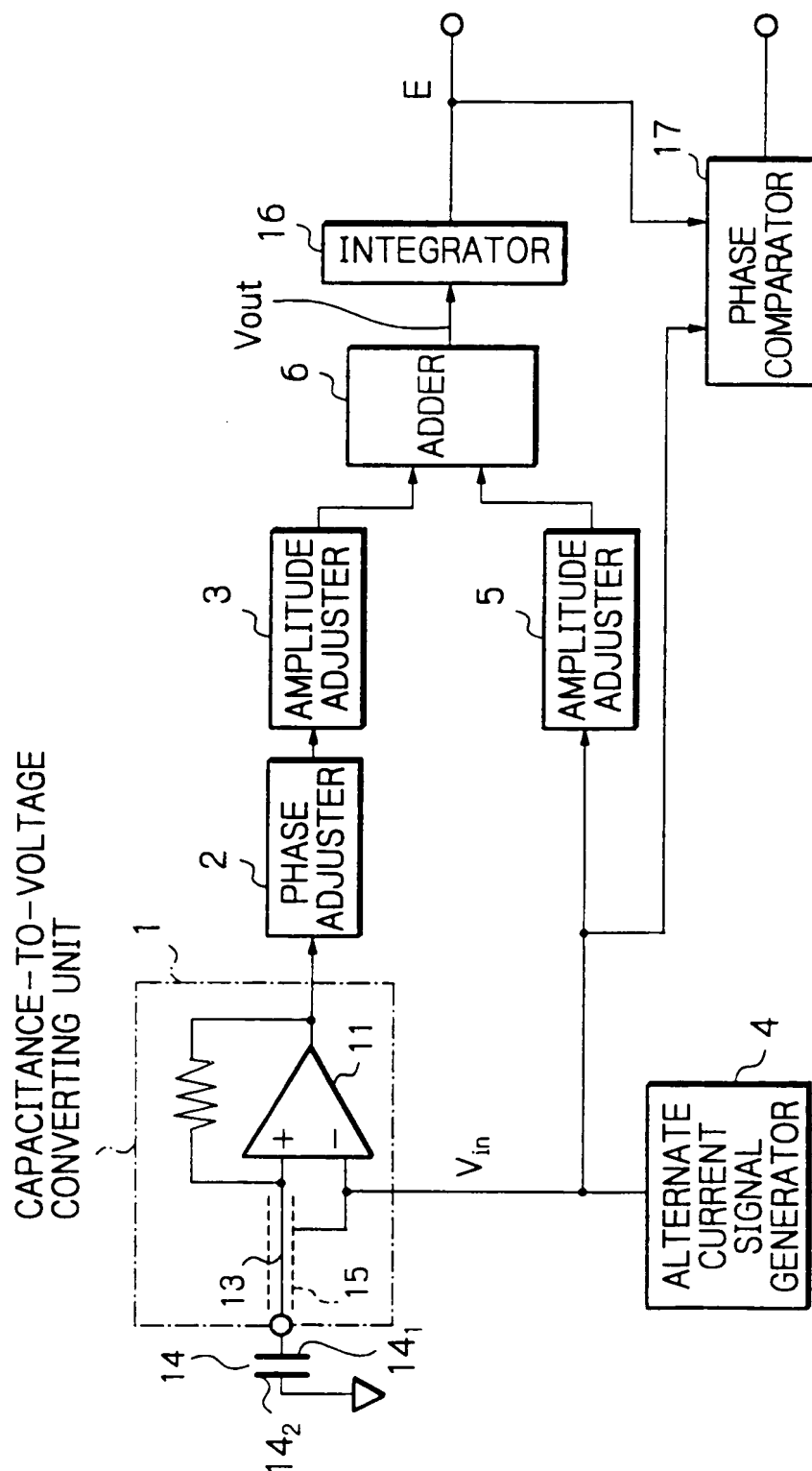


Fig. 6

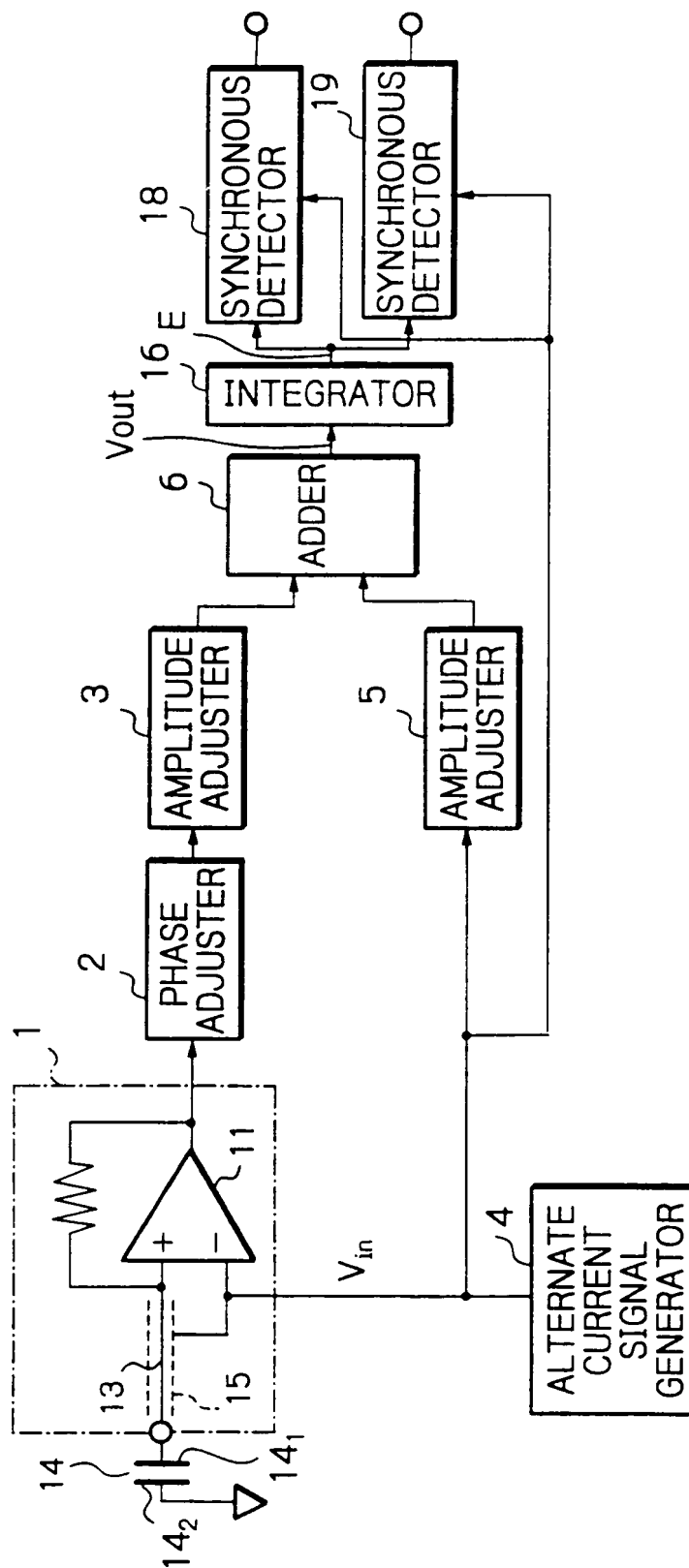


Fig. 7

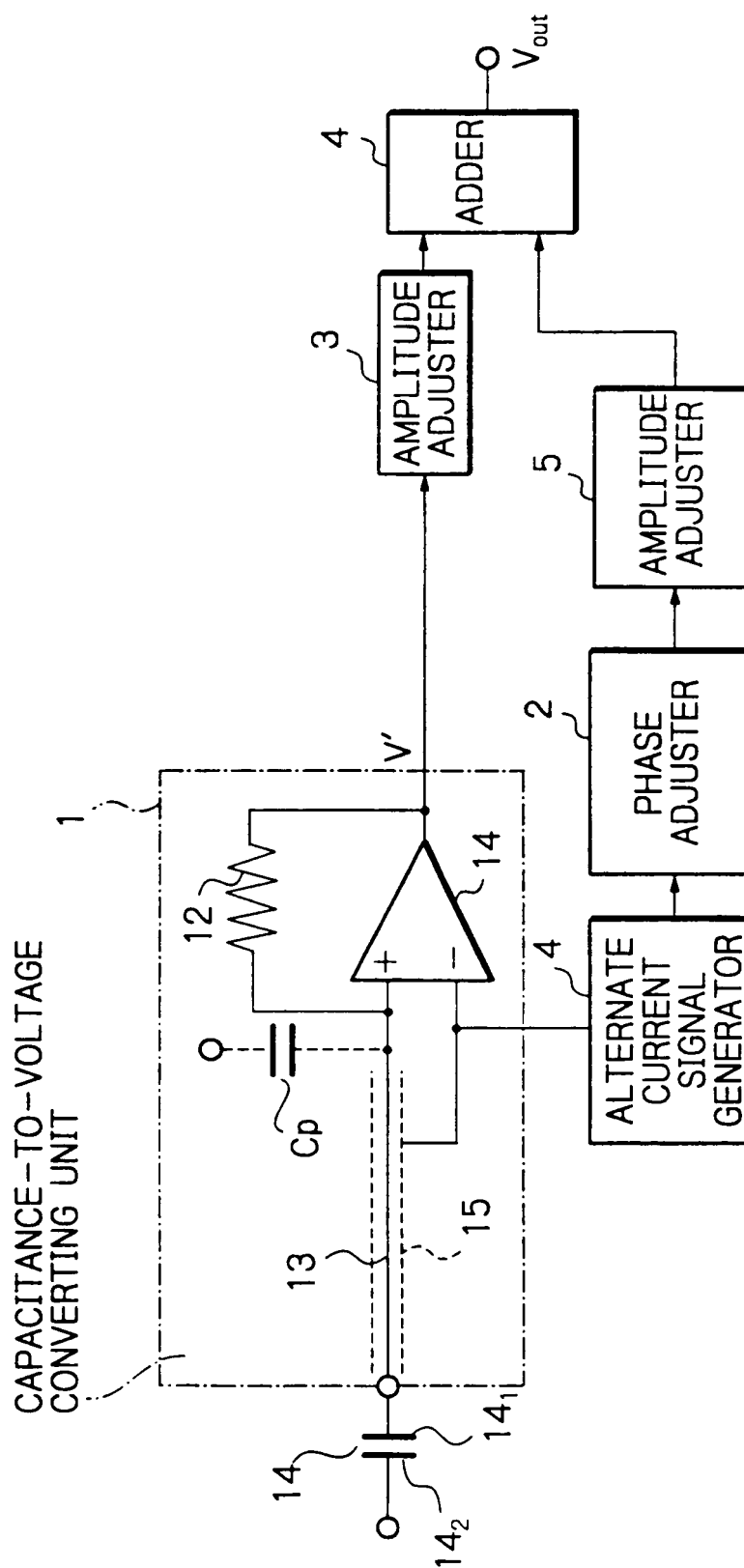


Fig. 8

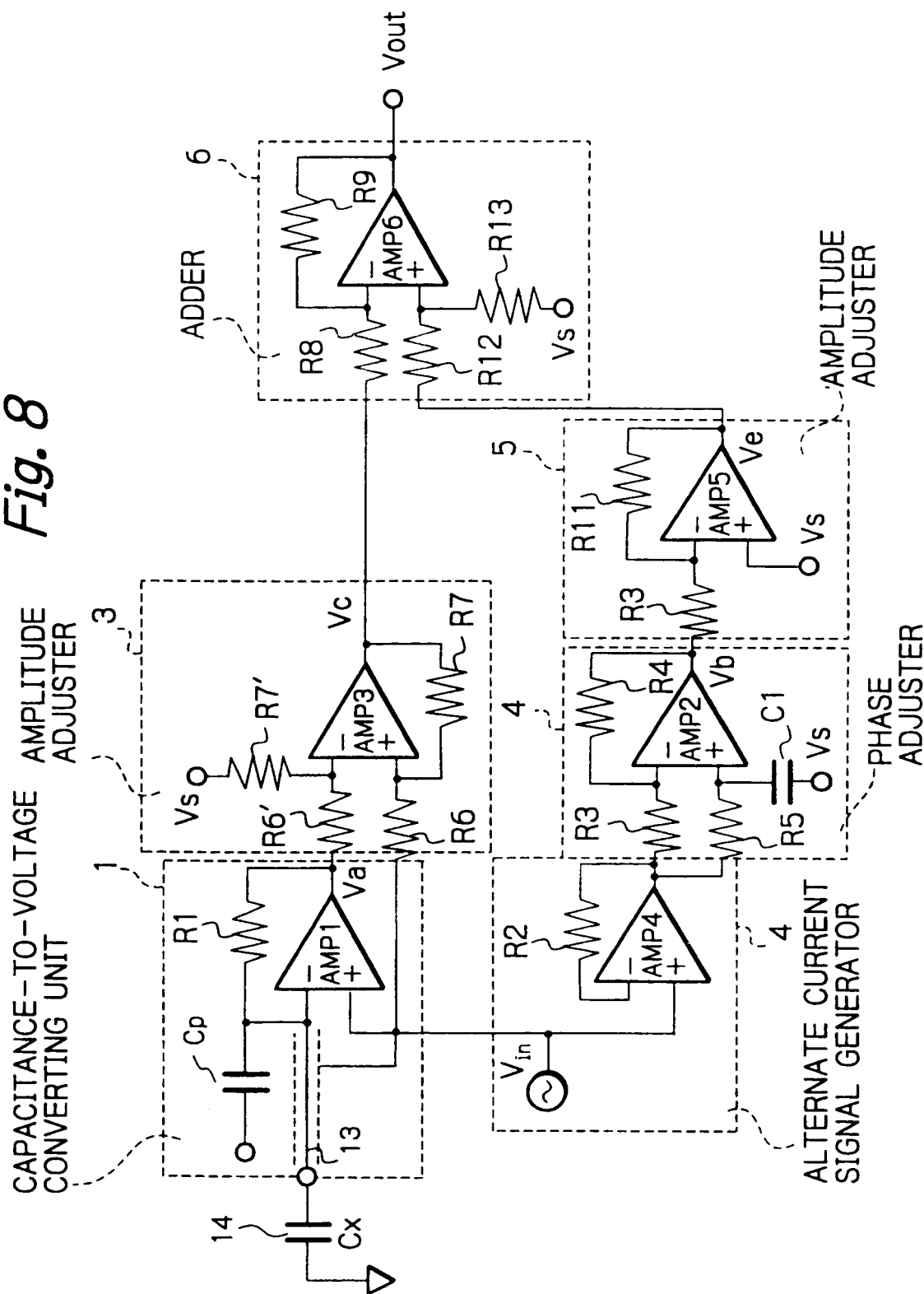


Fig. 9

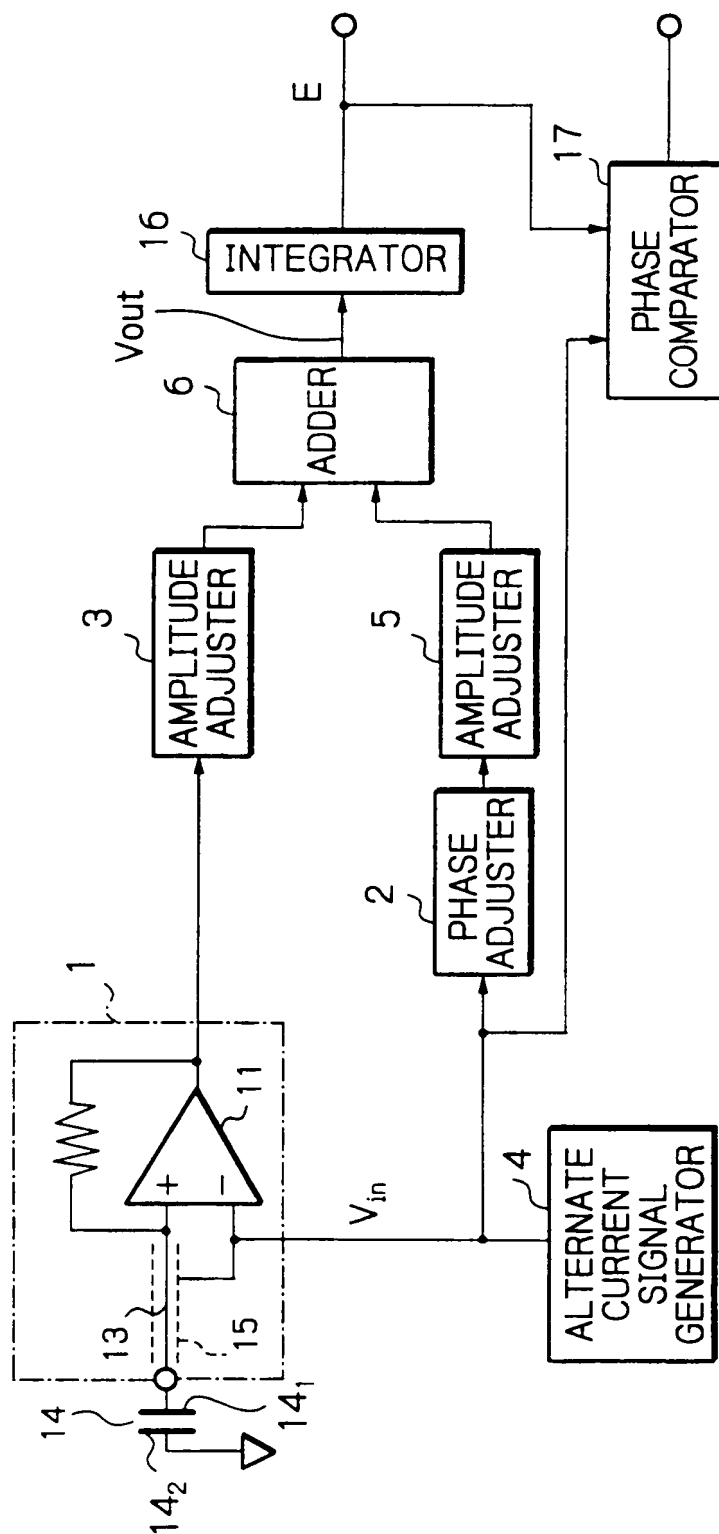


Fig. 10

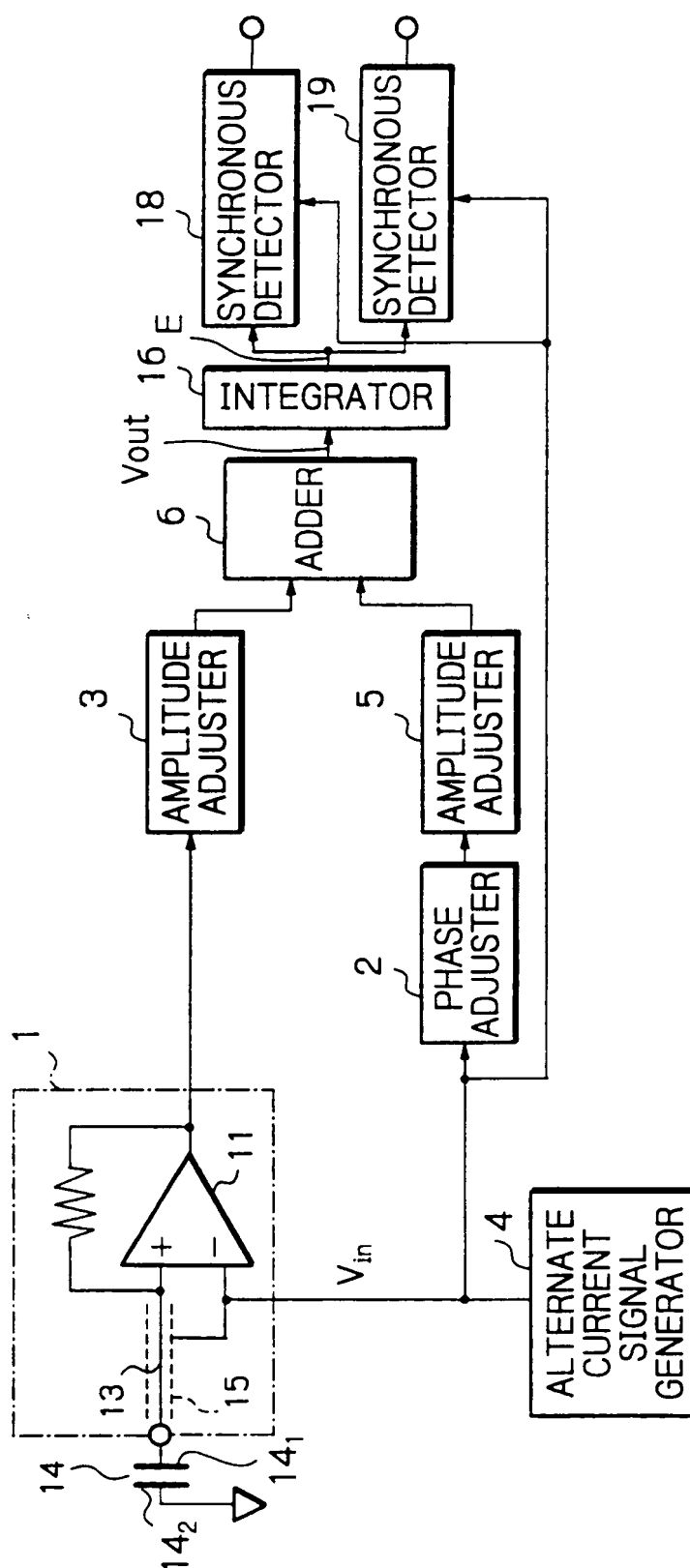
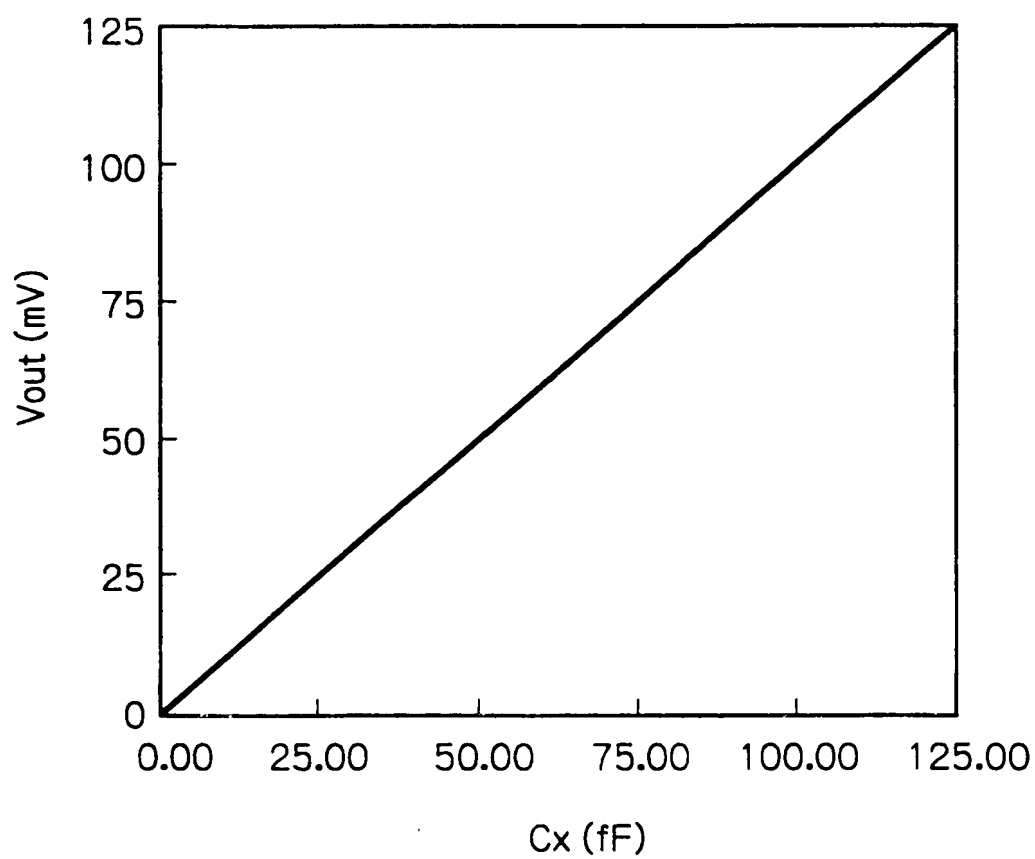


Fig. 11

INTERNATIONAL SEARCH REPORT

International Application No

PCT/JP 99/00229

A. CLASSIFICATION OF SUBJECT MATTER
IPC 6 G01R27/26

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC 6 G01R

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	PATENT ABSTRACTS OF JAPAN vol. 98, no. 2, 30 January 1998 & JP 09 280806 A (NISSAN MOTOR), 31 October 1997	1
A	see abstract	2, 9, 10, 12, 20, 21
Y	GB 2 020 816 A (MICRO-SENSORS INC.) 21 November 1979	1
A	see page 2, line 103 - line 111 see page 3, line 42 - line 65; figure 2	2, 12
A	US 4 918 376 A (PODUJE ET AL.) 17 April 1990 see column 3, line 1 - line 17; figure 1	1, 2, 12
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☒ Further documents are listed in the continuation of box C.

☒ Patent family members are listed in annex.

* Special categories of cited documents

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search

16 April 1999

Date of mailing of the international search report

03/05/1999

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INTERNATIONAL SEARCH REPORT

Inter. Application No

PCT/JP 99/00229

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	<p>MONTICELLI ET AL.: "OP-AMP CIRCUIT MEASURES DIODE-JUNCTION CAPACITANCE" ELECTRONICS. DE 1984 A 1985 : ELECTRONICS WEEK., vol. 48, no. 14, 10 July 1975, pages 112-113, XP002100006 NEW YORK US see the whole document -----</p>	

INTERNATIONAL SEARCH REPORT

information on patent family members

International Application No

PCT/JP 99/00229

Patent document cited in search report		Publication date	Patent family member(s)		Publication date
GB 2020816	A	21-11-1979	NONE		
<hr/>					
US 4918376	A	17-04-1990	JP	2068749 C	10-07-1996
			JP	7094964 B	11-10-1995
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